Notice of Allowability	Application No.	Applicant(s)	
	10/025,749	QUADER ET AL.	
	Examiner	Art Unit	
	Nam T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE and IDS filed on 9/24/04*.

2. ☒ The allowed claim(s) is/are *1-45*.

3. ☒ The drawings filed on *08 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/24/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *EAST SEARCH UPDATE*.

ANH PHUNG
PRIMARY EXAMINER

DETAILED ACTION

1. This is the response to the RCE and IDS filed on 9/24/04.

REASONS FOR ALLOWANCE

2. Claims 1-45 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to:

" determining whether all memory cells selected to store the first set of data bits have reached or exceeded the first predetermined threshold voltage level; if at least one memory cell selected to store the first set of data bits has not reached or exceeded the first predetermined threshold voltage level, continuing programming of uninhibited memory cells; if all memory cells selected to store the first set of data bits have reached or exceeded the first predetermined threshold voltage level, determining whether all memory cells selected to store second or third sets of data bits have reached or exceeded the first predetermined threshold voltage level; if at least one memory cell selected to store second or third sets of data bits has not reached or exceeded the first predetermined threshold voltage level, continuing programming uninhibited memory cells until all memory cells selected to store second or third sets of data bits have reached or exceeded the first predetermined threshold voltage level; and if all memory cells selected to store second or third sets of data bits have reached or exceeded the first

predetermined threshold voltage level, continuing programming all memory cells selected to store second or third sets of data bits" as claimed in the independent claim 1; or

" determining whether all memory cells selected to store the first predetermined charge level have reached or exceeded the first predetermined charge level; if at least one memory cell selected to store the first predetermined charge level has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells; if all memory cells selected to store the first predetermined charge level have reached or exceeded the first predetermined charge level, determining whether all memory cells selected to store second or third predetermined charge levels have reached or exceeded the first predetermined charge level; and if at least one memory cell selected to store second or third predetermined charge levels has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells until all memory cells selected to store second or third predetermined charge levels have reached or exceeded the first predetermined charge level" as claimed in the independent claim 20; or

" simultaneously storing charge in the first, second and third sets of memory cells; continuing storing charge in the memory cells if no memory cell has reached or exceeded the first predetermined charge level; inhibiting storing charge of any memory cell in the first, second and third sets that has reached or exceeded the first predetermined charge level; determining whether all memory cells in the first set have reached or exceeded the first predetermined charge level; and if at least one memory cell in the first set has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells" as claimed in the independent claim 23; or

" determining whether all memory cells selected to store the first set of data bits have reached or exceeded the first predetermined threshold voltage level; if at least one memory cell selected to store the first set of data bits has not reached or exceeded the first predetermined threshold voltage level, continuing programming of uninhibited memory cells; if all memory cells selected to store the first set of data bits have reached or exceeded the first predetermined threshold voltage level, determining whether any memory cell has reached or exceeded a second predetermined threshold voltage level, the second predetermined threshold voltage level representing a second set of data bits; and inhibiting programming of any memory cell that has reached or exceeded the second predetermined threshold voltage level and continuing programming of uninhibited memory cells" as claimed in the independent claim 25; or

" determining whether all memory cells selected to store the first predetermined charge level have reached or exceeded the first predetermined charge level; if at least one memory cell selected to store the first predetermined charge level has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells; if all memory cells selected to store the first predetermined charge level have reached or exceeded the first predetermined charge level, determining whether any memory cell selected to store second or third predetermined charge levels has reached or exceeded the second predetermined charge level; inhibiting storing charge in any memory cell that has reached or exceeded the second predetermined charge level; and if no memory cell selected to store second or third predetermined charge levels has reached or exceeded the second predetermined charge level, continuing storing charge in uninhibited memory cells" as claimed in the independent claim 27; or

" simultaneously storing charge in the first, second and third sets of memory cells; continuing storing charge in the memory cells if no memory cell has reached or exceeded the first predetermined charge level; inhibiting charging of any memory cell in the first, second and third sets that has reached or exceeded the first predetermined charge level; determining whether all memory cells in the first set have reached or exceeded the first predetermined charge level; if at least one memory cell in the first set has not reached or exceeded the first predetermined charge level, continuing storing charge in uninhibited memory cells; if all memory cells in the first set have reached or exceeded the first predetermined charge level, determining whether any memory cell in the second set has reached or exceeded the second predetermined charge level; and if at least one memory cell in the second set has not reached or exceeded the second predetermined charge level, continuing storing charge in uninhibited memory cells in the second and third sets" as claimed in the independent claim 30; or

" a second set of one or more memory cells selected to store a charge equal to or greater than a second predetermined charge level corresponding to a second set of data bits, wherein the memory device is configured to simultaneously program the first and second sets of memory cells and inhibit programming of any memory cell that reaches or exceeds the first predetermined charge level until all memory cells in the first set have reached or exceeded the first predetermined charge level" as claimed in the independent claim 31; or

" inhibiting storing charge in any memory cell that has reached or exceeded the first predetermined charge level; determining whether all memory cells in the first set of memory cells have reached or exceeded the first predetermined charge level; if at least one memory cell in the first set has not reached or exceeded the first predetermined charge level, continuing

storing charge in uninhibited memory cells; and if all memory cells in the first set have reached or exceeded the first predetermined charge level, continuing storing charge in the first set of memory cells" as claimed in the independent claim 39; or

" terminating application of the programming conditions to individual ones of the plurality of memory cells designated for the first and second threshold levels as the cells designated for the first and second threshold levels individually reach said first threshold level; after those of the memory cells designated for the first threshold level have all reached the first threshold level, applying programming conditions to those of the plurality of memory cells designated for the second threshold level; and terminating application of the programming conditions to individual ones of the plurality of memory cells designated for the second threshold level as the cells designated for the second threshold level individually reach said second threshold level" as claimed in the independent claim 41; or

" a second set of one or more memory cells selected to store a charge equal to or greater than a second predetermined charge level corresponding to a second set of data bits, wherein the memory device is configured to simultaneously program the first and second sets of memory cells and inhibit programming of any memory cell that reaches or exceeds the first predetermined charge level until all memory cells in the first set have reached or exceeded the first predetermined charge level" as claimed in the independent claim 44.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nam T Nguyen whose telephone number is 571-272-1878. The examiner can normally be reached on 8 am to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Nam T Nguyen
Examiner
Art Unit 2824

4/28/05

ANH PHUNG
PRIMARY EXAMINER